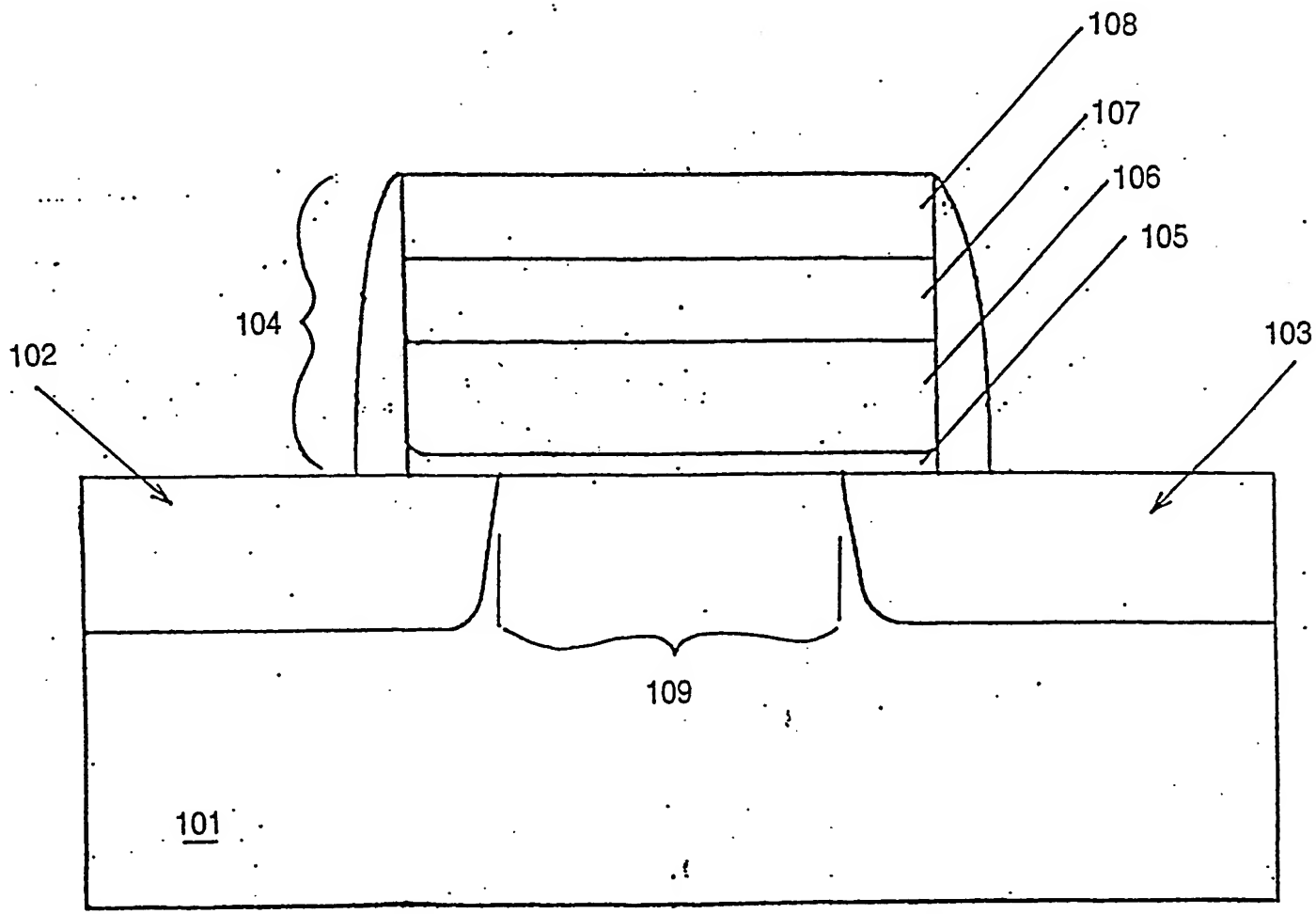
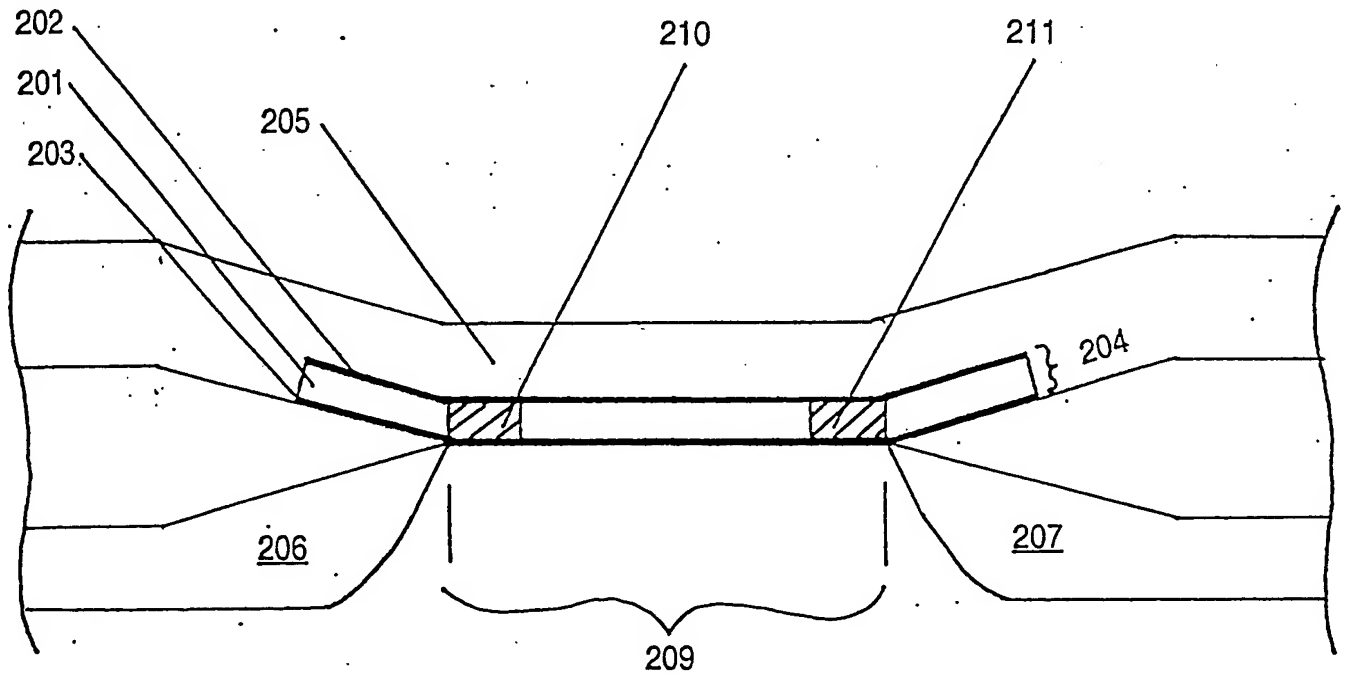
100

FIGURE 1
(PRIOR ART)



200

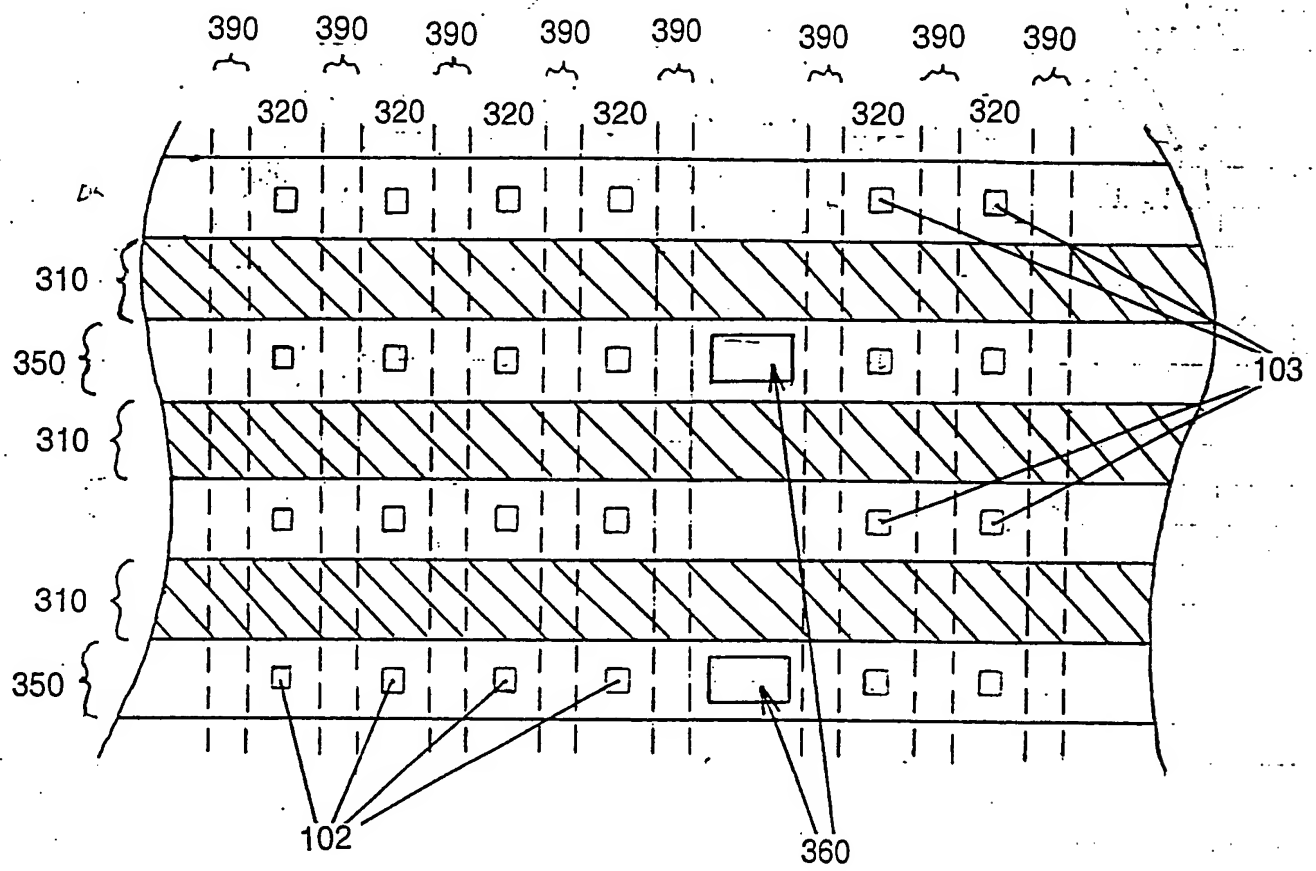
FIGURE 2
(PRIOR ART)



300

FIGURE 3

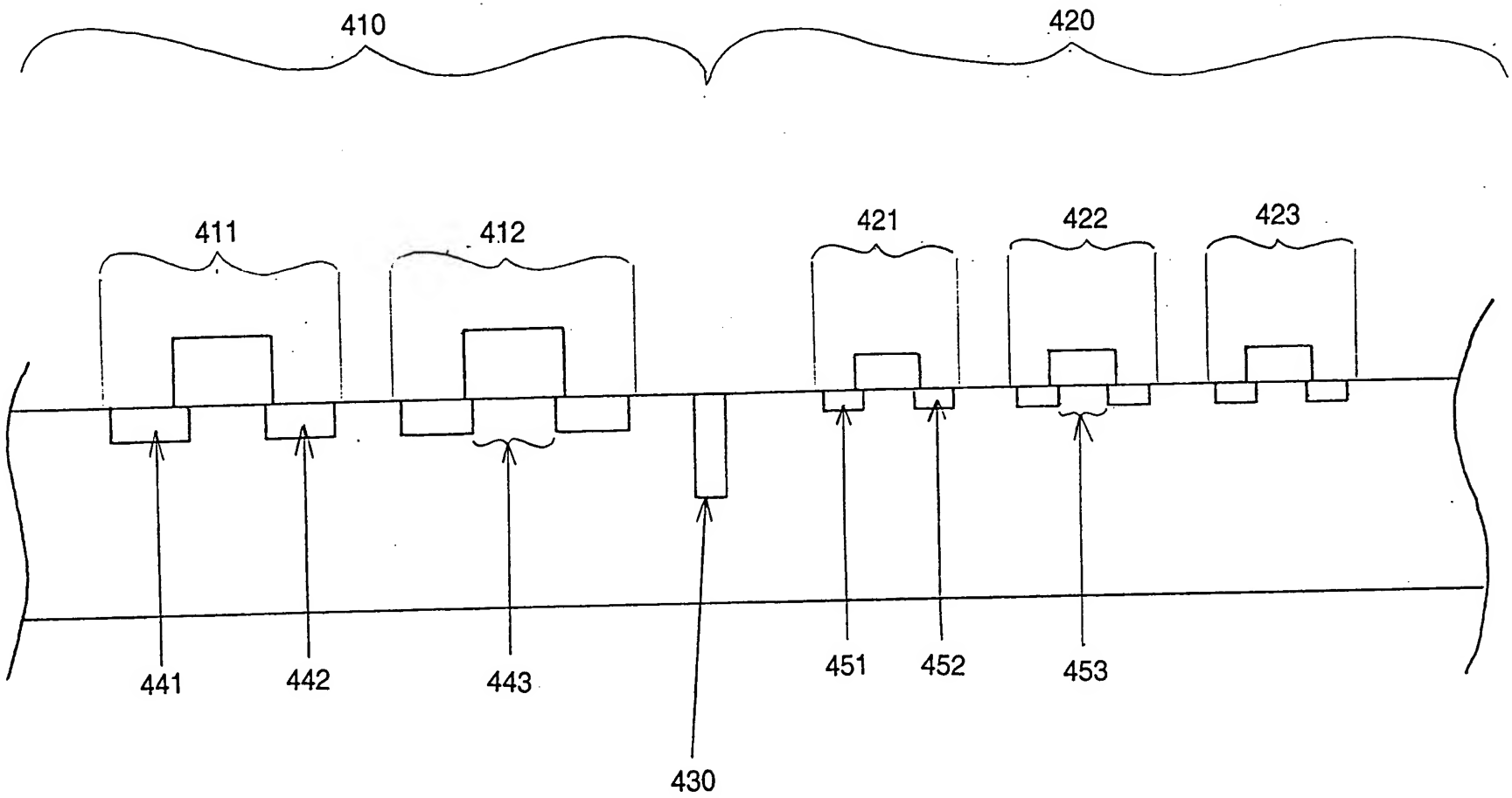
(PRIOR ART)



STAEDTLER®
Engineer's Computation Pad

FIGURE 4

400



Engineer's Computation Pad
STADTLER

500

FIGURE 5

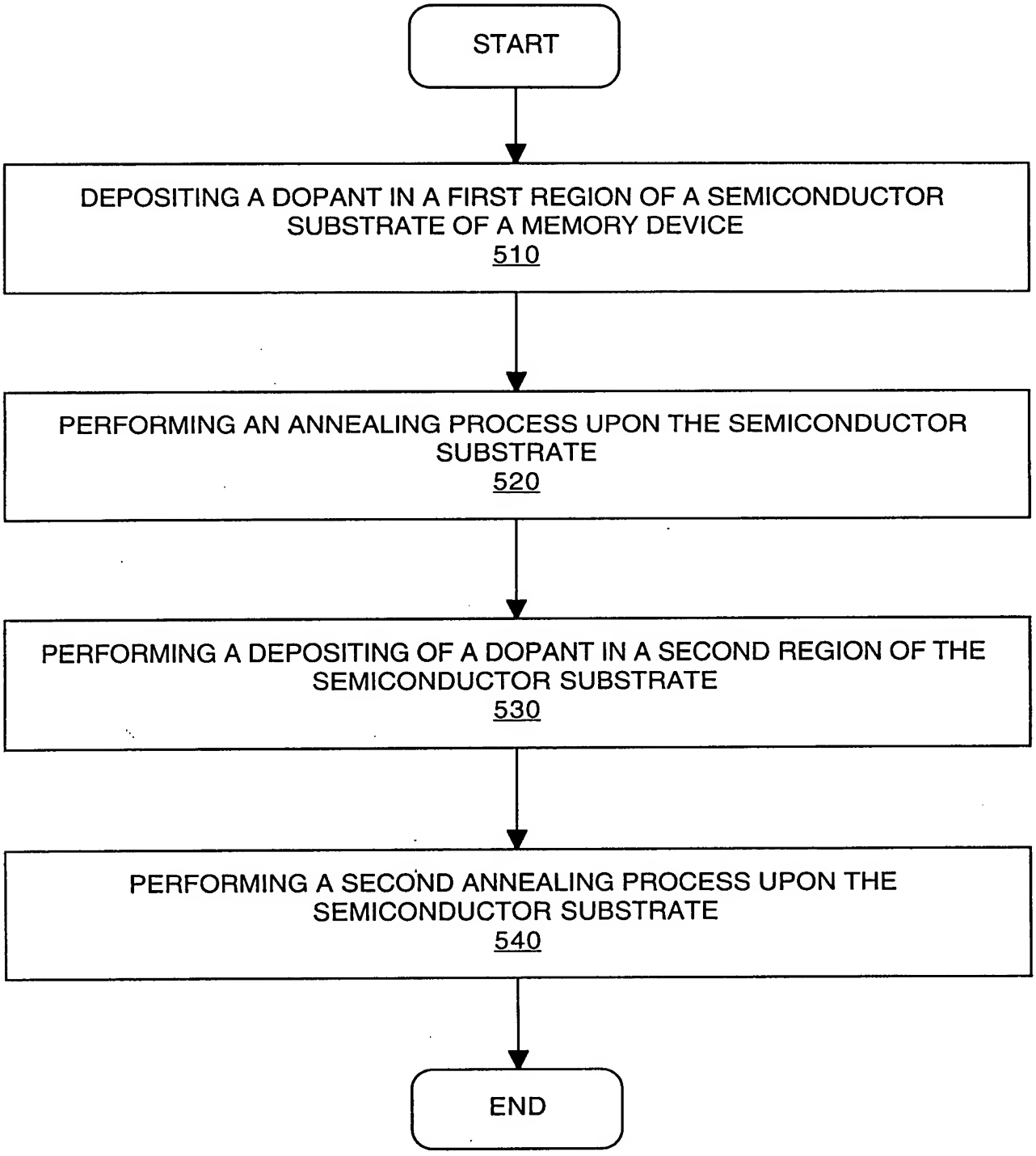

START
DEPOSITING A DOPANT IN A FIRST REGION OF A SEMICONDUCTOR SUBSTRATE OF A MEMORY DEVICE
510
PERFORMING AN ANNEALING PROCESS UPON THE SEMICONDUCTOR SUBSTRATE
520
PERFORMING A DEPOSITING OF A DOPANT IN A SECOND REGION OF THE SEMICONDUCTOR SUBSTRATE
530
PERFORMING A SECOND ANNEALING PROCESS UPON THE SEMICONDUCTOR SUBSTRATE
540
END

FIGURE 6A

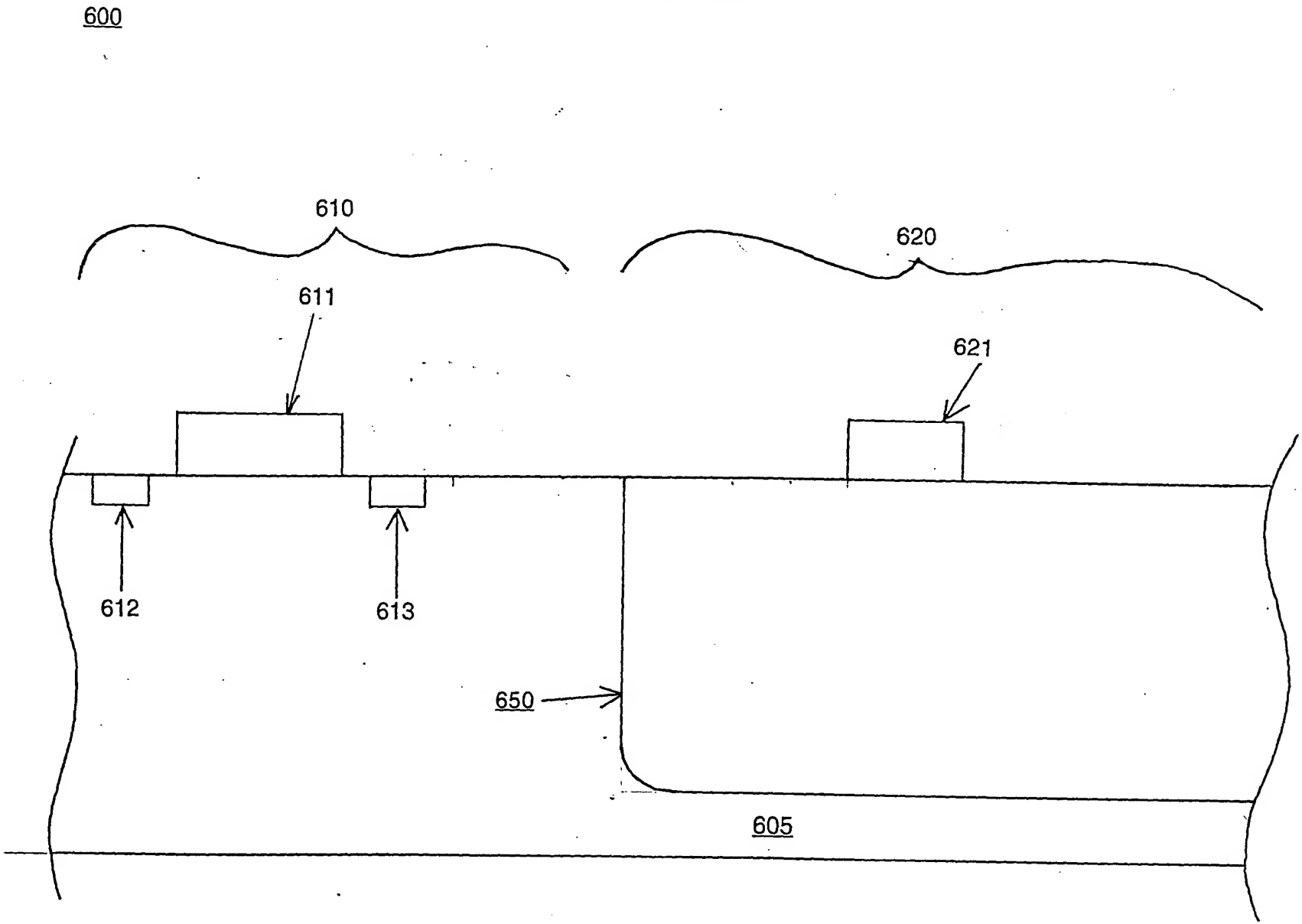
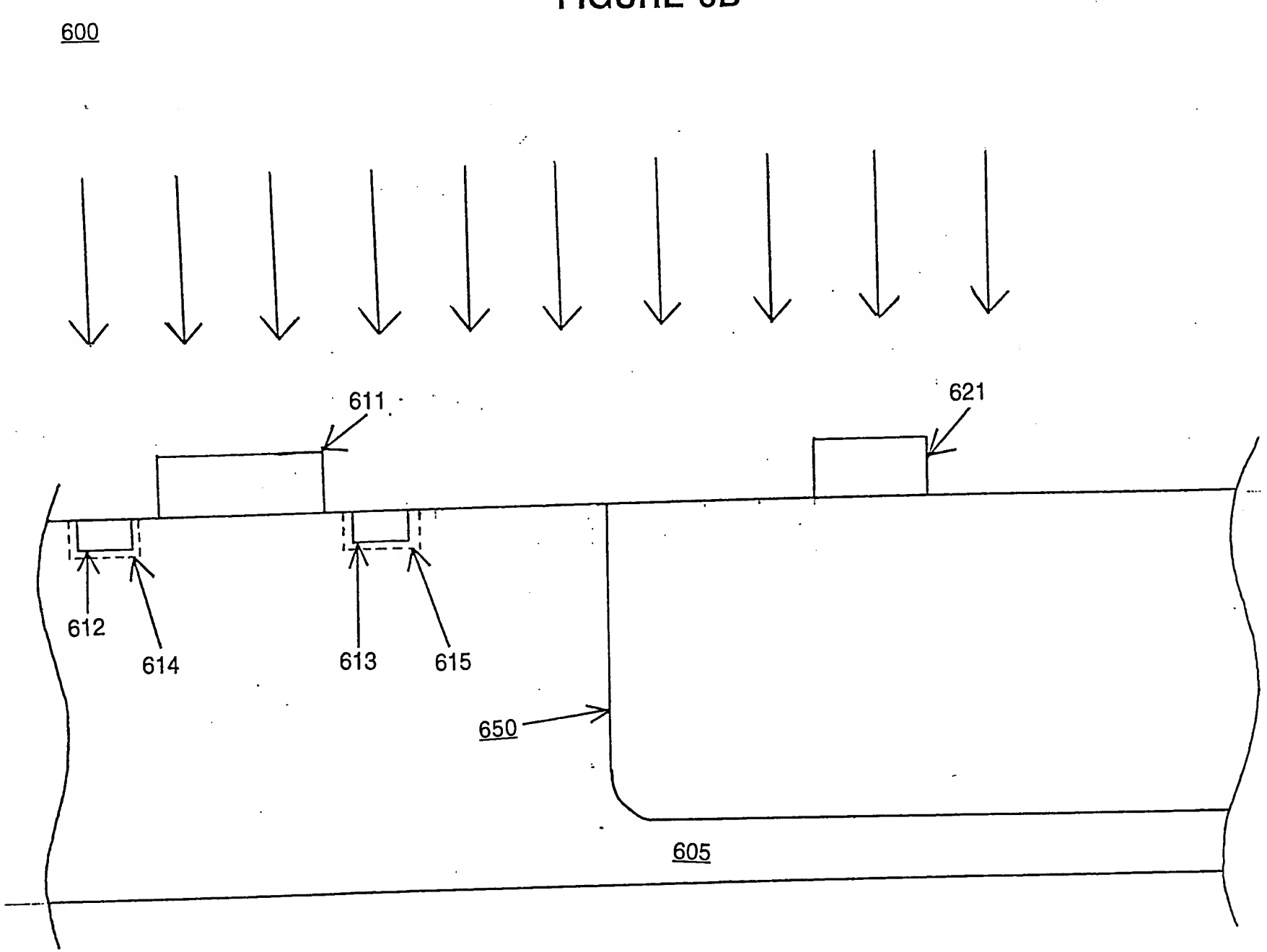
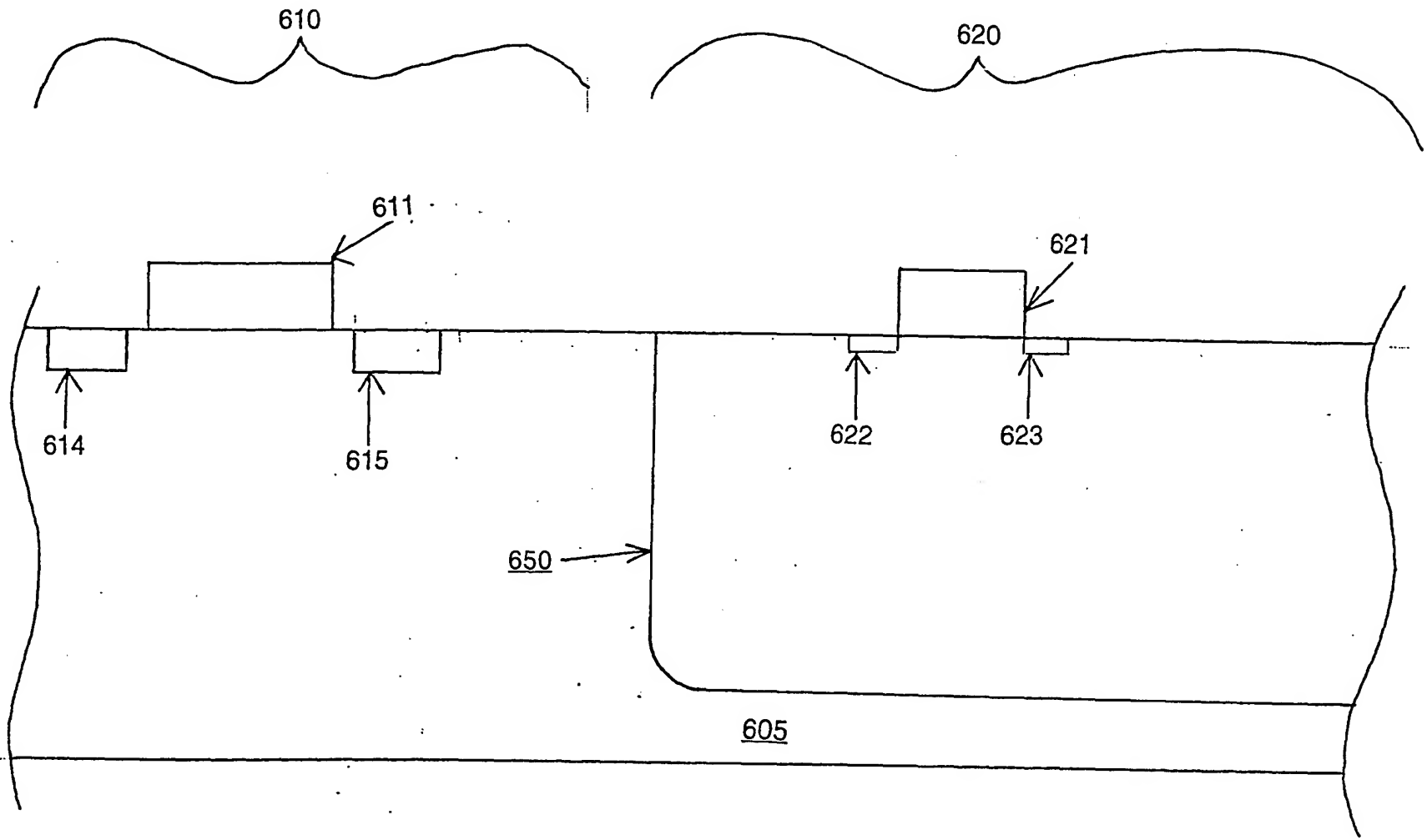


FIGURE 6B



600

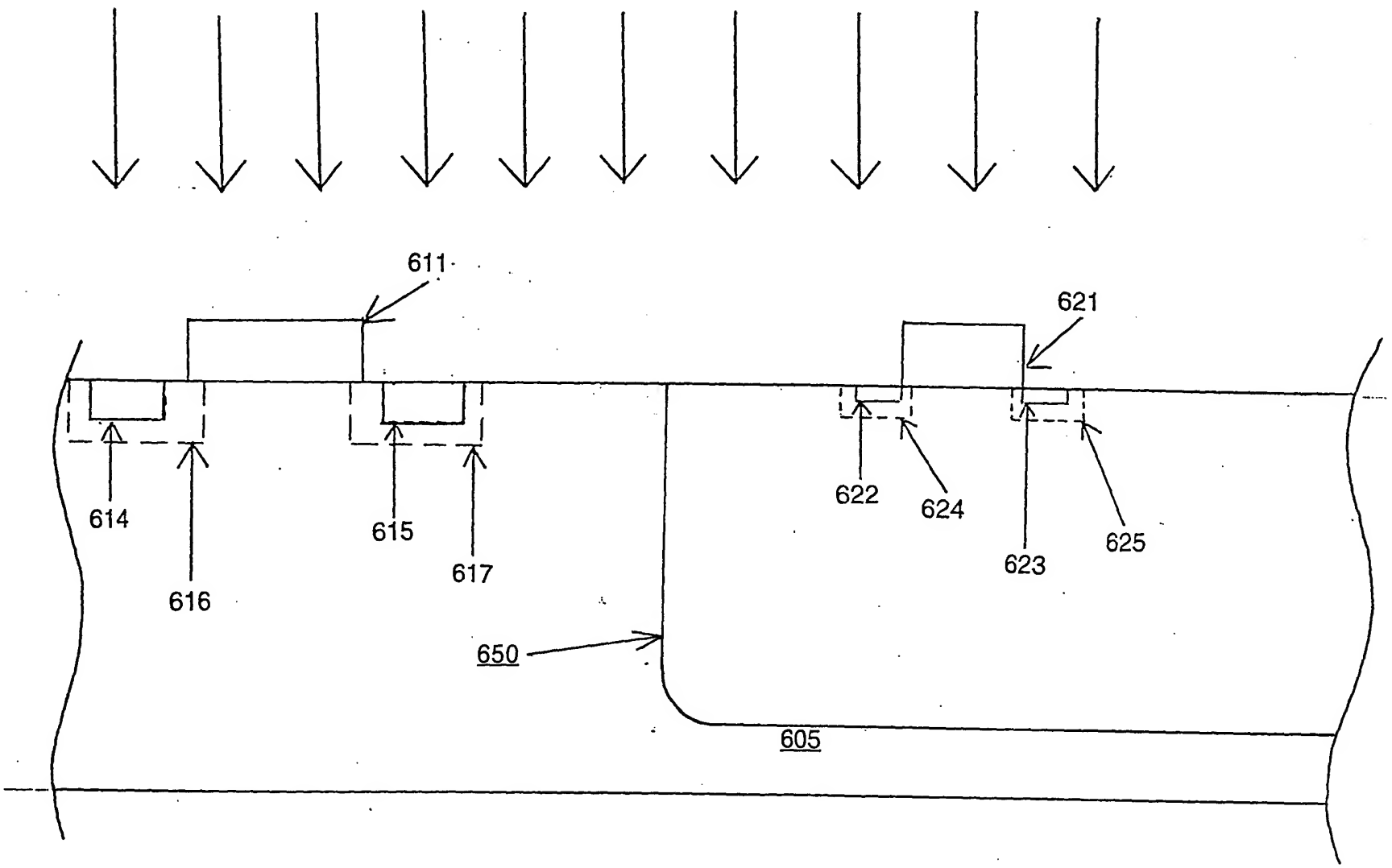
FIGURE 6C



Engineer's Computation Pad

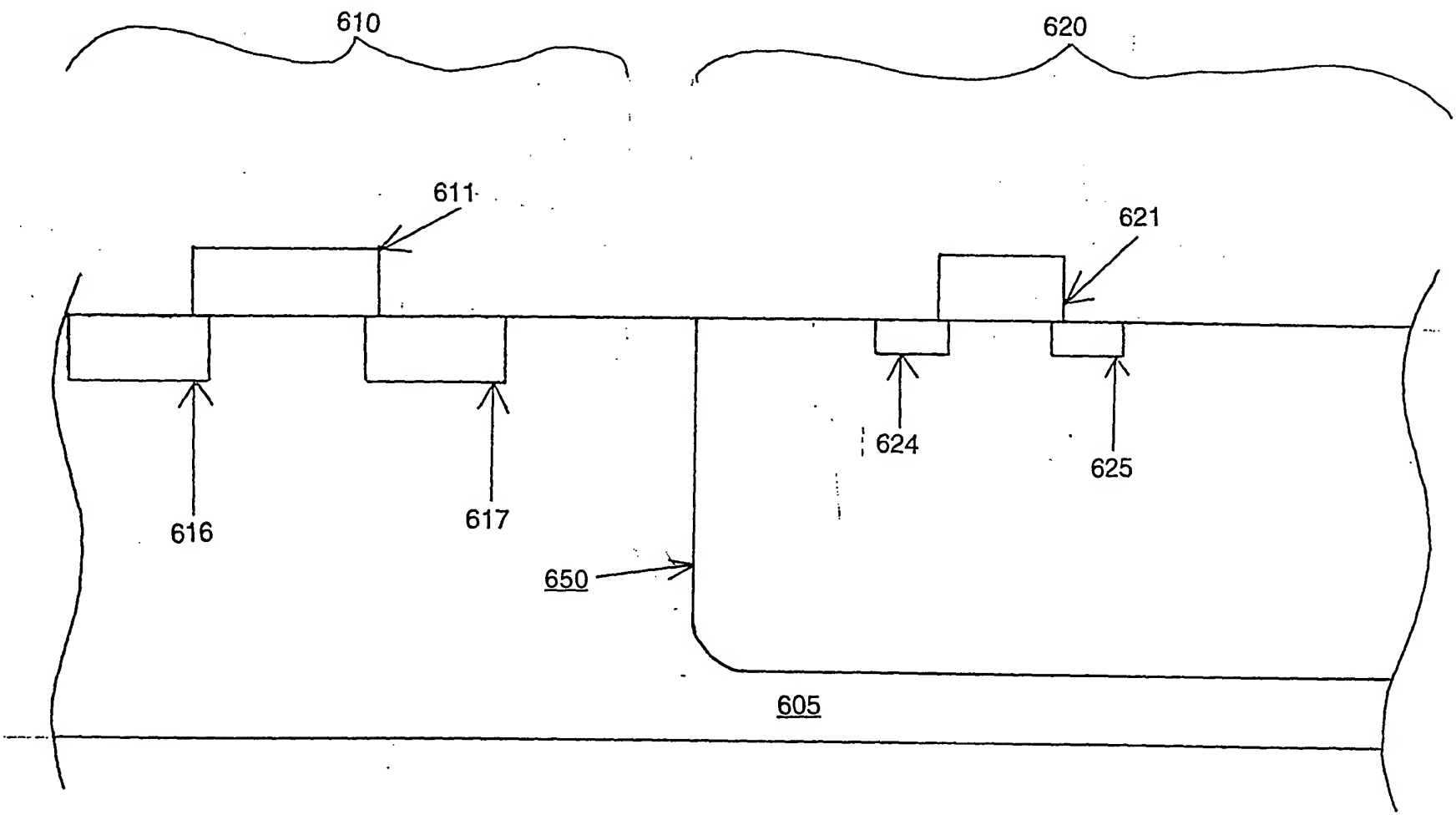
600

FIGURE 6D



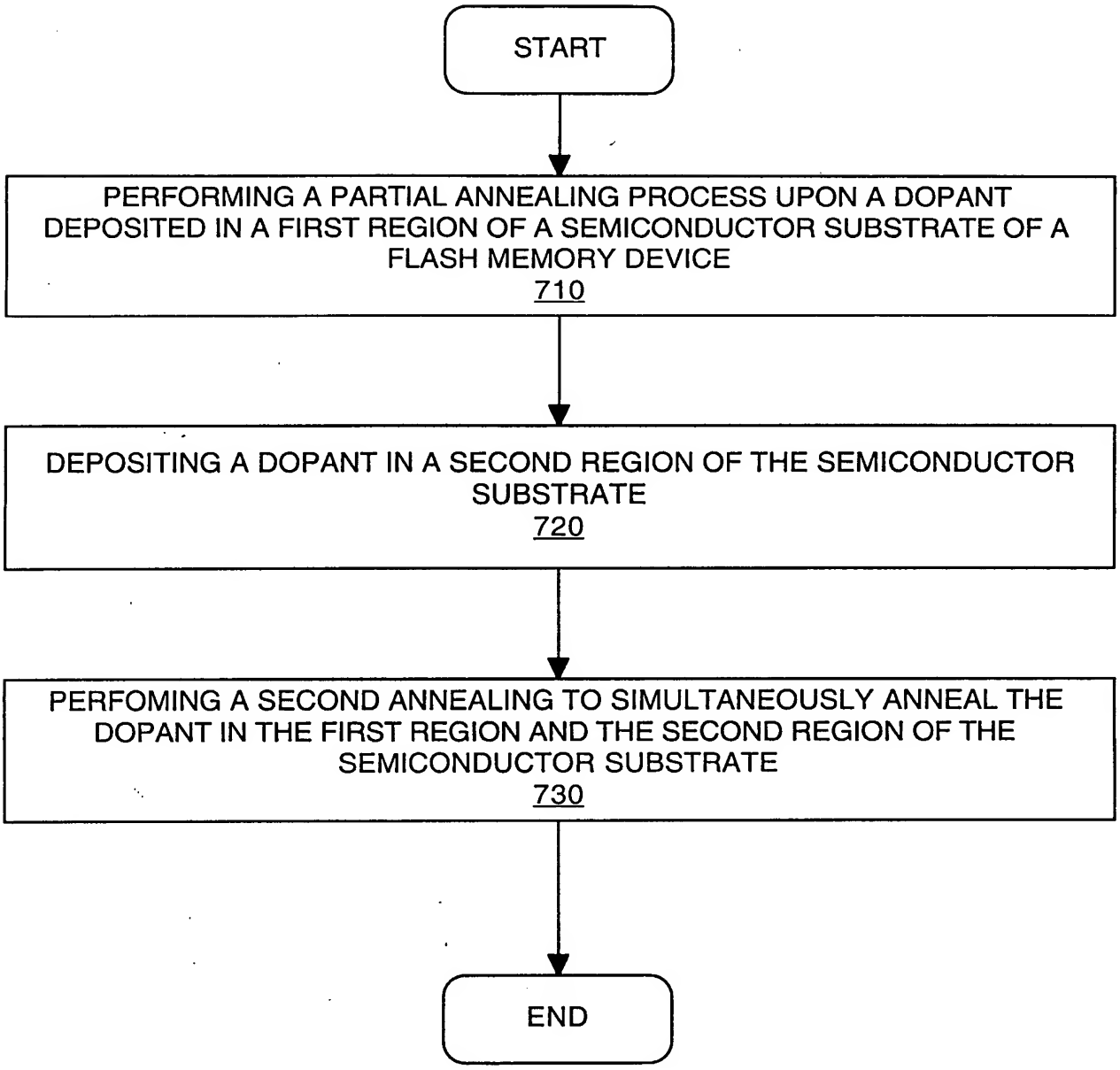
Engineer's Computation rac

FIGURE 6E



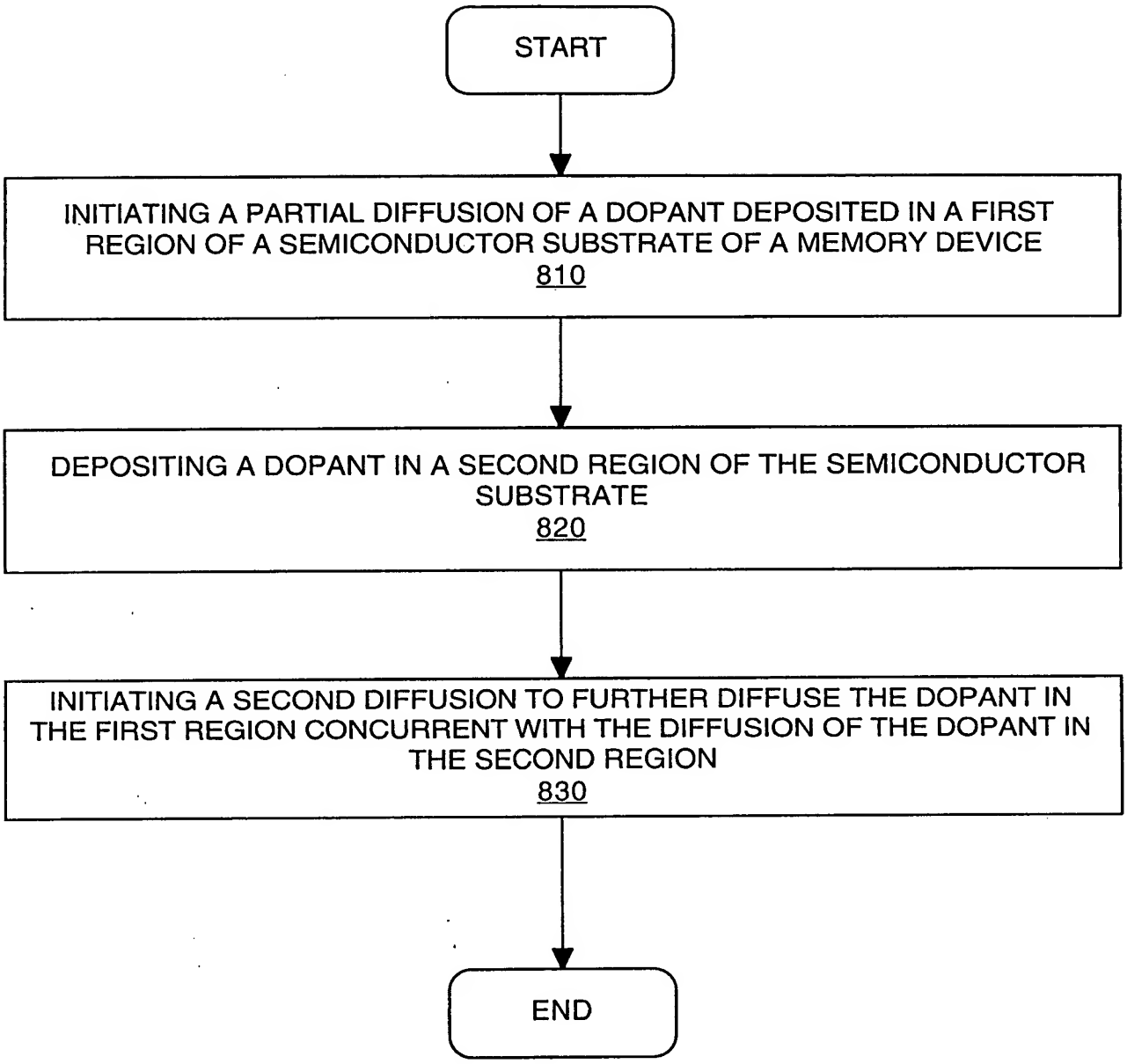
700

FIGURE 7


START
PERFORMING A PARTIAL ANNEALING PROCESS UPON A DOPANT DEPOSITED IN A FIRST REGION OF A SEMICONDUCTOR SUBSTRATE OF A FLASH MEMORY DEVICE
710
DEPOSITING A DOPANT IN A SECOND REGION OF THE SEMICONDUCTOR SUBSTRATE
720
PERFOMING A SECOND ANNEALING TO SIMULTANEOUSLY ANNEAL THE DOPANT IN THE FIRST REGION AND THE SECOND REGION OF THE SEMICONDUCTOR SUBSTRATE
730
END

800

FIGURE 8


START
INITIATING A PARTIAL DIFFUSION OF A DOPANT DEPOSITED IN A FIRST REGION OF A SEMICONDUCTOR SUBSTRATE OF A MEMORY DEVICE
810
DEPOSITING A DOPANT IN A SECOND REGION OF THE SEMICONDUCTOR SUBSTRATE
820
INITIATING A SECOND DIFFUSION TO FURTHER DIFFUSE THE DOPANT IN THE FIRST REGION CONCURRENT WITH THE DIFFUSION OF THE DOPANT IN THE SECOND REGION
830
END